Space Preliminary Evaluation Testing of Advanced Piezo on Insulator Technology

Kaoutar Zeljami [(1)], Aintzane Lujambio [(1)], Mario Rueda [(1)], Sylvain Ballandras [(2)], Thierry Laroche [(2)]
Emilie Courjon[(2)], Florent Bernard[(2)], Alexandre Raveski[(2)]

[(1)]ALTER
Calle Tomás Alva Edison, 4
41092, Sevilla - Spain
Email:kaoutar.zeljami@altertechnology.com

[(2)]SOITEC
TEMIS Innovation 18 Rue Alain Savary,
25000 Besançon - France
Email:sylvain.ballandras@soitec.com

INTRODUCTION

Surface Acoustic Wave (SAW) filters are key components in modern wireless communication systems, including smartphones, Internet-of-Things (IoT) devices, and satellite communication payloads, where they provide highly selective frequency filtering while maintaining compact size while minimizing payload, low mass, and low power consumption. Their operation relies on the piezoelectric effect, enabling efficient signal processing and effective mitigation of electromagnetic interference. While SAW technology has reached a high level of maturity for terrestrial applications, the increasing demand for high-performance and cost-effective RF front-end solutions in space systems creates new challenges regarding power handling capability, thermal stability, reliability, and qualification for harsh operating environments. Furthermore, the multiplication of satellites in particular for Low-Earth Orbit (LEO) application requires significant payload reduction which can be potentially addressed by the SAW technology, provided it can meet Space standards.

To address these challenges, the HOMEMADE project aims to develop and qualify a new generation of SAW filters based on Piezoelectric-On-Insulator (POI) [1] technology for space applications, targeting a Technology Readiness Level (TRL) of 7. The proposed solutions are intended to satisfy the stringent performance and reliability requirements of both geostationary and Low Earth Orbit (LEO) satellite constellations, supporting the growing demand for next-generation space communication infrastructures. In addition to the qualification of SAW devices for space use, the project investigates the potential of advanced substrate technologies capable of extending the performance limits of conventional SAW filter implementations.

Among the most promising approaches, POI substrates have recently attracted considerable attention due to their ability to enhance the performance of acoustic devices [2]. Conventional SAW and temperature-compensated SAW (TC-SAW) technologies have been widely deployed in the frequency range from 500 MHz to 2.5 GHz; however, their performance can be constrained by limitations in temperature stability, power handling capability, and insertion loss due to the limited coupling and quality factors. By combining a thin piezoelectric layer with an engineered insulating substrate, POI structures offer improved acoustic confinement and thermal properties, enabling enhanced device performance. In particular, POI-based SAW resonators, which constitute the fundamental building blocks of RF filters, have demonstrated the potential to achieve high quality factors (Q), strong electromechanical coupling, improved thermal behavior, and superior power handling capability. These characteristics position POI-SAW technology as a strong candidate for future high-performance RF filtering applications in both terrestrial and space environments.

In this paper, we are focusing on single-port resonators built on improved POI structures using new trap rich layer to enhance SAW figure of Merit (FoMs) on such substrates. Single-port synchronous resonators actually provide a representative and efficient platform for evaluating the intrinsic properties of the acoustic structure and predicting the achievable performance of future filter designs. Consequently, this work presents a preliminary evaluation of advanced POI technology through the fabrication, assembly, and characterization of a set of POI-based SAW resonators. The preliminary evaluation focuses on the key parameters required for future space-qualified filtering solutions, including RF performance, temperature stability, and power handling capability. Furthermore, dedicated temperature and power step-stress tests were conducted to investigate device robustness under representative operating conditions.

The devices were evaluated in accordance with [3] ESCC 2263502 adapted to the specific characteristics of SAW components, and ESCC Generic Specification for SAW filter Hermetically sealed [4]. The results provide an initial assessment of the suitability of POI technology for future spaceborne SAW filters and establish the basis for subsequent qualification activities and filter-level developments within the HOMEMADE project.

POI TECHNOLOGY OVERVIEW

Modern Surface Acoustic wave (SAW) filters are widely taking advantage of POI substrates [2] to address current and coming generations of telecommunication standards. POI is advantageously combining a single crystal layer of $LiTaO_3$ or $LiNbO_3$ transferred on a Si-based substrate using the Smart-Cut™ technique [1] adapted to this piezoelectric material and bonded using a silicon dioxide SiO2-layer-based molecular adhesion [1]. Pure shear waves are classically excited on top of the resulting compound substrates using interdigitated transducers (IDT) classically composed of Aluminum-Copper electrode gratings. The introduction of the so-called trap-rich layer [1] between the SiO2 layer and Si substrate significantly reduces the effect of parasitic surface conduction (PSC) [5] which pumps and dissipates energy from the mode. As a consequence, all FoMs of the exploited mode are significantly boosted by these breakthrough wave-guides which are particularly offering coupling factors and reflection coefficients both in excess of 10 % and Q factors as high as 5000 at 2 GHz. Fig 1 recalls the basic structure of POI wafers. The Smart Cut™ technology is used to define a single-crystal layer transferred onto a Silicon substrate using a hydrophilic molecular bonding process implying a Silicon Dioxide layer. This SiO2 layer is grown by PECVD on the Si substrate equipped with the so-called trap-rich layer which consists of a Poly-Silicon layer grown by LPCVD, exhibiting a thickness of 500 nm or 1µm according to SOITEC manufacturing rules and standards. Typical SiO2 and LiTaO3 layer thicknesses are in the 300 nm - 1.0 µm range according to SOITEC thickness control rules.

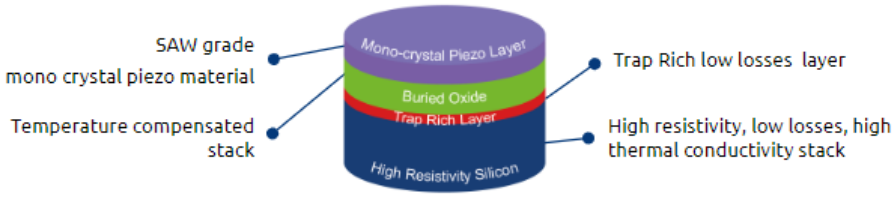


Fig 1. Typical structure of a POI substrate, combining a top piezoelectric layer on a Buried Oxide atop a Si base substrate equipped with a trap-rich layer and role of each stack element

This wafer archetype is declined in various forms combining either lithium tantalate or lithium niobate for frequency domains known as Low-Band (LB, 500 MHz - 1 GHz), Mid-High Band (MHB, 1 - 3 GHz) and Ultra-High Band (UHB, above 3 GHz). The most popular piezoelectric cut angles are 42° for $LiTaO_3$ and 36° for $LiNbO_3$, although other cuts close to these may be used to fine tune some SAW properties (coupling, TCF, others). In the above defined standard POI configuration, we noted a Si(100) crystal orientation. The alignment of the Si base and LiTaO3 layer flats plays a major role in the control of the spurious contributions. Si(111) substrates also can be advantageously used, in particular to control spurious contributions depending on the targeted frequency range [6].

Improving the quality of the POI substrate and subsequently the shear mode FoMs can be achieved by optimizing the different stack layers. Changing the composition of the Trap-Rich layer was identified as one of the most promising routes for that purpose.

DEVICE DESIGN AND PERFORMANCES

The devices to be tested consisted of several samples of single port SAW resonators operating near 1.6 GHz with IDT of 120 finger pairs and two reflecting mirrors each equipped with 20 electrodes and 40λ aperture resonators at pitches p = 1.2 µm as shown in Fig 2. Metal thickness was fixed to 150 nm of AlCu|2%.

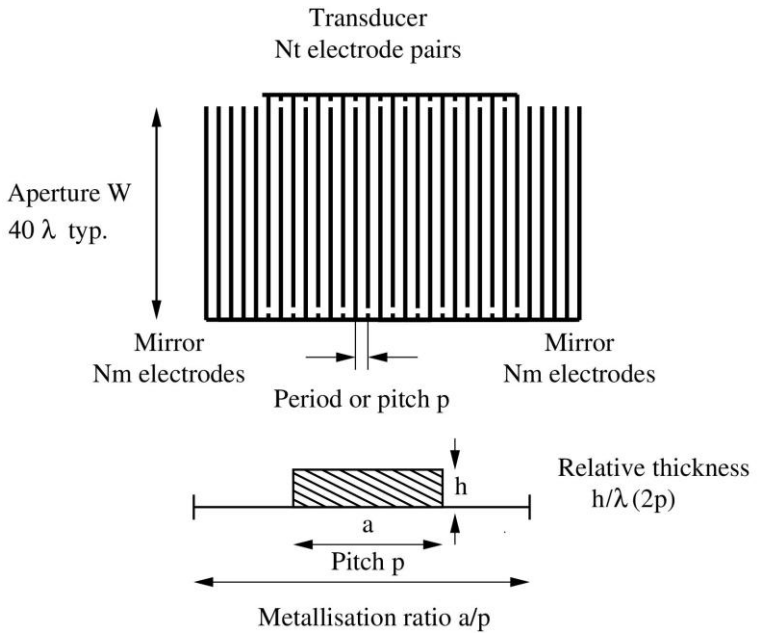


Fig 2. Principle Structure of the single port synchronous resonator test-vehicle, definition of the electrode critical dimensions.

The following tables summarize the figures of merit (FoM) to consider for the resonators to be tested. These are the key characteristics such as resonance frequency, quality factors, and coupling coefficient.

TABLE I. Figures of merit (FoM) to consider for the resonators to be tested

New Trap-Rich - W92		f_{res} (MHz)	f_{Ares} (MHz)	Q_{res}	Q_{Ares}	Q_{Bode}(fit)	K_s^2(%)
Embedding	mean	1596.3	1671.8	319.3	2708.3	2403.8	8.83
	Std	0.807	0.557	29.8	428.8	22.3	$4.1x10^{-2}$
De-Embedding	mean	1602.8	1674.0	990.0	2073.3	3960.3	8.32
	std	7.2996.e-01	0.628	171.8	182.8	88.1	$2.9x10^{-2}$

New Trap-Rich - W93		f_{res} (MHz)	f_{Ares} (MHz)	Q_{res}	Q_{Ares}	Q_{Bode}(fit)	K_s^2(%)
Embedding	mean	1597.7	1672.4	285.4	1788.7	2403.3	8.727
	Std	0.512	0.567	42.6	77.1	30.5	$2.3x10^{-2}$
De-Embedding	mean	1604.2	1674.5	745.2	2933.1	3757.8	8.22
	std	0.554	0.542	134.6	260.3	75.2	$1.3x10^{-2}$

The resonators will be assembled in the 3.8SQ package with the die size 1.6×1.1mm^2. Fig 3 depicts the drawings of the package and the assembly that will be performed. One can note that the device is composed of IDT and mirror electrodes connected to contact pads via metal tracks that can affect the RF measurement of the resonator response. Therefore, a de-embedding process has to be applied to access the actual device figures of merit, providing objective means to selectivity compare the resonator electroacoustic properties from one wafer to another.

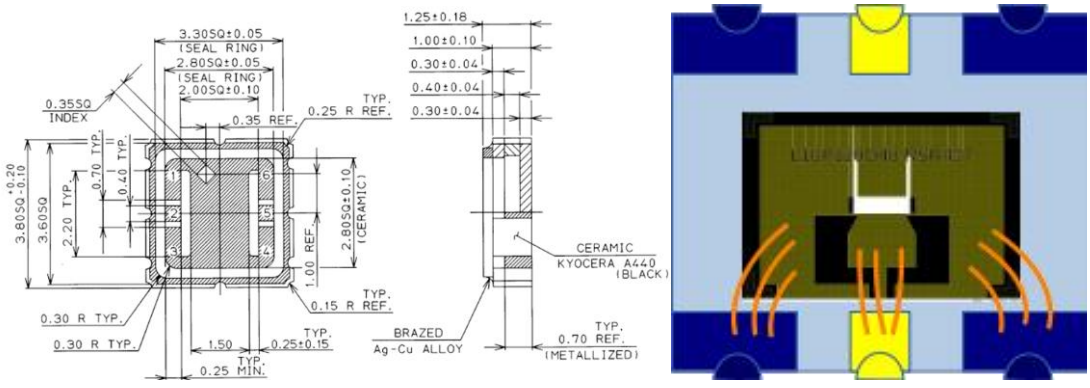


Fig 3. The 3.8SQ package (left) and assembly (right) drawings

In addition to the devices under test, open and short structures will be also assembled in the same package to de-embed the performance of the resonators from the complete structure.

SPACE PRELIMINARY EVALUATION TESTING

Device description

This section describes the preliminary evaluation testing activities conducted at ALTER TECHNOLOGY on the advanced new POI technology. The assessment was performed on a limited number of samples of a SAW resonator test structure as the main element for filters, referenced as RSR437 and developed by SOITEC, assembled in a 3.8SQ package configuration. The objective of this evaluation is to provide an initial characterization of the RF performance and robustness of advanced POI technology, with respect to its potential suitability for space applications. The test campaign included RF performance characterization, as well as temperature-step and power-step stress testing, aimed at investigating device behavior under progressively increasing RF power conditions.

The evaluation test flow was defined in accordance with [3] ESCC 2263502 and was tailored to address the specific characteristics of the RSR437 resonator devices. As mentioned before, devices to be tested following this document are selected to be several samples of a one port SAW resonator RSR437 (SOITEC nomenclature) with Interdigitated Transducer IDT of 120 fingers and two reflecting mirrors each equipped with 20 electrodes. depicts the drawings of the package used and the assembly that will be performed.

The SAW resonators are composed of IDT and mirror electrodes connected to contact pads via metal tracks that can affect the RF measurement of the resonator response. Therefore, a de-embedding process had to be applied using open and short structures to access the actual device figures of merit, providing objective means to selectively compare the resonator electrostatic properties from one wafer to another. To carry out all the electrical tests, samples were soldered onto dedicated test boards designed for the testing purpose. The test board is made of RO4350B with a 20mil thickness, featuring a 50-ohm grounded coplanar waveguide and SMA connectors operating up to 18 GHz. Fig 4 shows the picture of the soldered sample as well as the open and short standard.

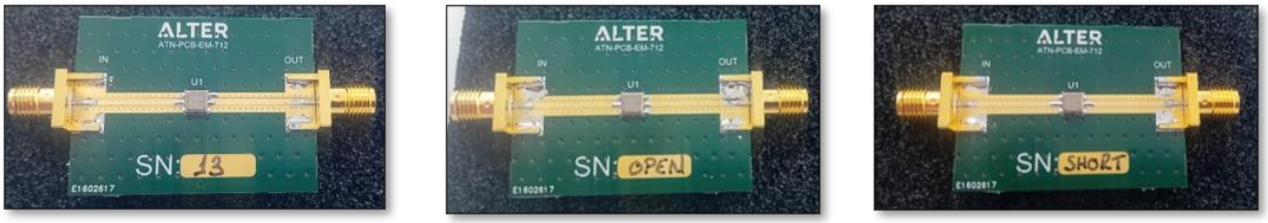


Fig 4. PCB for testing SAW resonators, featuring a soldered device under test, with open–short de-embedding standard

Testing flow

All samples underwent an initial non-destructive inspection, consisting of an External Visual Inspection (EVI), during which no anomalies were detected. Following this an Electrical testing was conducted to characterize the resonator response over a wide temperature range and to evaluate their ability to withstand various power-stress conditions, with particular emphasis on assessing performance improvements in these aspects.

The testing procedures were designed to intentionally overstress specific resonator characteristics to identify potential failure modes. If device failure occurs during step-stress testing, a failure analysis would be performed to investigate possible design, fabrication, or material-related defects affecting device reliability. This approach aims to identify potential device weaknesses and provide guidance for future design improvements. The testing flow agreed within the project is shown in Fig 5.

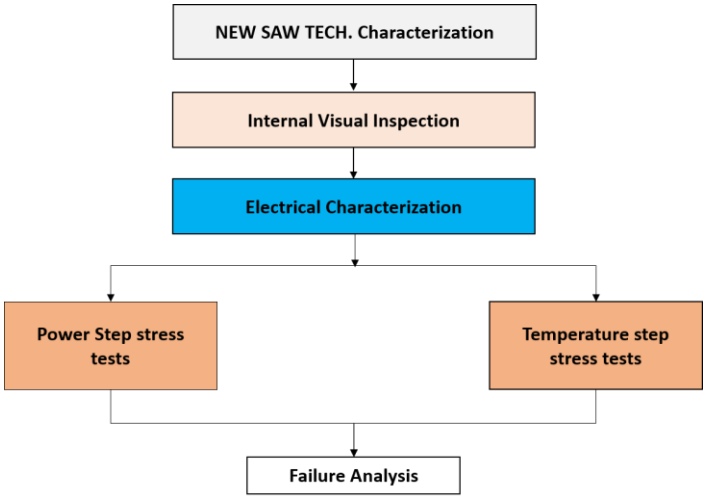


Fig 5. Evaluation test sequence for SAW resonators built on the new substrates

EVALUATION RESULTS

Temperature step stress tests (TST)

The objective of the Temperature Step Stress (TST) campaign is to assess the stability of the resonator response under progressively increasing temperature conditions and to identify potential performance degradation mechanisms under representative operating conditions. The devices were operated at a constant input power level (-10 dBm at resonance frequency) for 16 hours at each temperature step, ranging from moderate to elevated temperatures. After each stress step, the samples were returned to room temperature, allowed to stabilize, and subsequently re-characterized through electrical measurements (EMRT) to evaluate any irreversible changes in performance in device performance. The procedure is graphically described in Fig 6 .

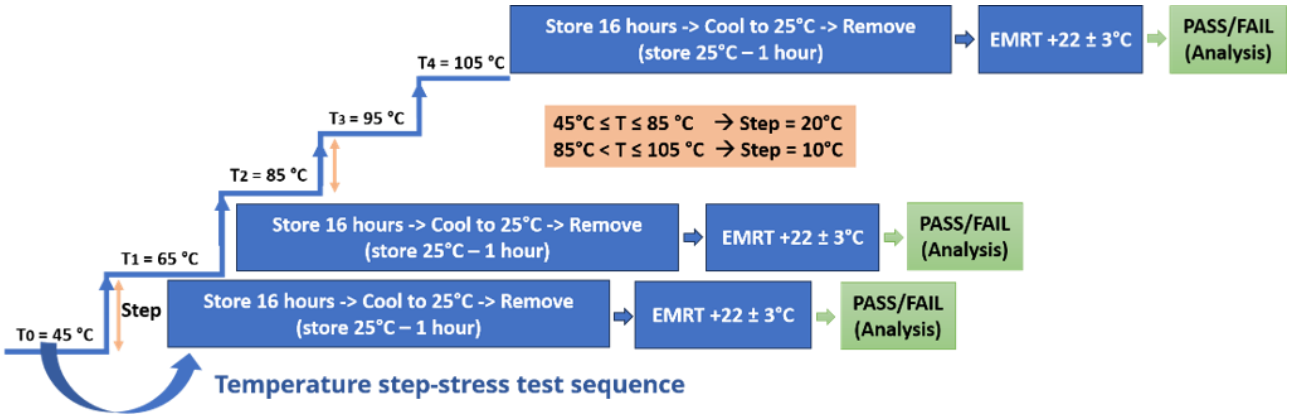


Fig 6. Temperature step-stress test sequence

Fig 7 presents the S_{11} response of a representative device measured at different stages of the temperature stress sequence. The results show a strong overlap of the resonator response across all temperature steps, indicating highly stable behavior and the absence of significant drift or degradation within the applied stress range.

The slight variations observed remain within the expected measurement repeatability and do not indicate any measurable performance degradation. From the measured S_{11} responses, key resonator figures of merit were extracted using a MATLAB-based post-processing tool, including resonant and anti-resonant frequencies, quality factors, and electromechanical coupling coefficient. The extraction methodology also incorporates open and short de-embedding standards to ensure accurate characterization of the intrinsic device response. Overall, the TST results demonstrate robust resonator behavior under thermal stress conditions, with no evidence of irreversible performance degradation.

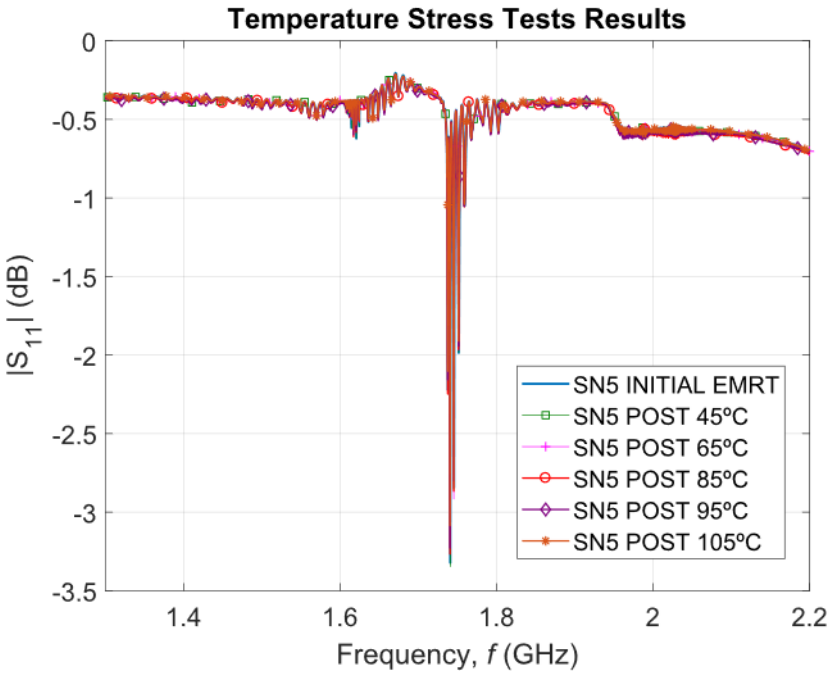


Fig 7. Temperature step-stress test sequence S_{11} measurements during temperature step-stress testing, shown for the initial step (blue), after 45 °C (square), 65 °C (+), 85 °C (circle), 95 °C (diamond), and final measurement after 105 °C (*)

Power step stress tests (PST)

The Power Step Stress (PST) campaign was conducted to evaluate the resonator robustness under increasing RF power excitation at elevated temperature conditions. The applied temperature during PST corresponds to the maximum temperature reached during the TST campaign, ensuring a worst-case combined stress scenario.

During the test, RF input power was progressively increased in controlled steps while maintaining a constant operating frequency near the resonance peak, where electromechanical coupling efficiency is maximized. This methodology allows isolation of power-induced degradation mechanisms without additional thermal variation effects. Power levels range between -20dBm and +30dBm following the procedure described in TABLE II .

TABLE II. Conditions for power step-stress test.

POWER STEP STRESS TEST			
Conditions	**Initial value**	**Step**	**Final value**
Power	-20 dBm	-20 dBm ≤ Pin ≤ +10 dBm → 10 dB +10 dBm < Pin ≤ +20 dBm → 5 dB +20 dBm < Pin ≤ +30 dBm → 2 dB	≤ 30 dBm
Duration	30 min for each power value		
Temperature	Maximum temperature obtained after TST		
Frequency	f_{Res}		

After each power step, the devices were returned to room temperature and re-characterized using S_{11} measurements. Fig 8 show the picture of the sample inside the chamber for PST process.

Fig 9 shows the S_{11} response of a representative sample at different stages of the PST sequence. The measured responses exhibit a high degree of overlap across all power levels, indicating stable resonator operation under increasing RF excitation. The absence of noticeable shifts in the resonance profile suggests that the device maintains stable electromechanical behavior even under elevated power conditions. As in the TST campaign, resonator parameters were extracted from the measured S_{11} data using the same de-embedding and post-processing methodology.

No anomalous behavior or degradation trends were observed throughout the full power stress sequence, confirming stable device operation within the tested range.



Fig 8. Pictures of the samples inside the test chamber for PST process

Following the defined test procedure, electrical measurements at room temperature have been performed after each power step level. Fig 9 shows the S_{11} measurements of one sample at some steps of the whole PST process. These results prove that the performance of the samples tested remained stable throughout all test conditions, confirming their ability to operate reliably at the maximum power applied. Two samples have been submitted to the power step stress test in total; however, this graph highlights the results of one selected sample (SN4) for greater clarity in the visualization.

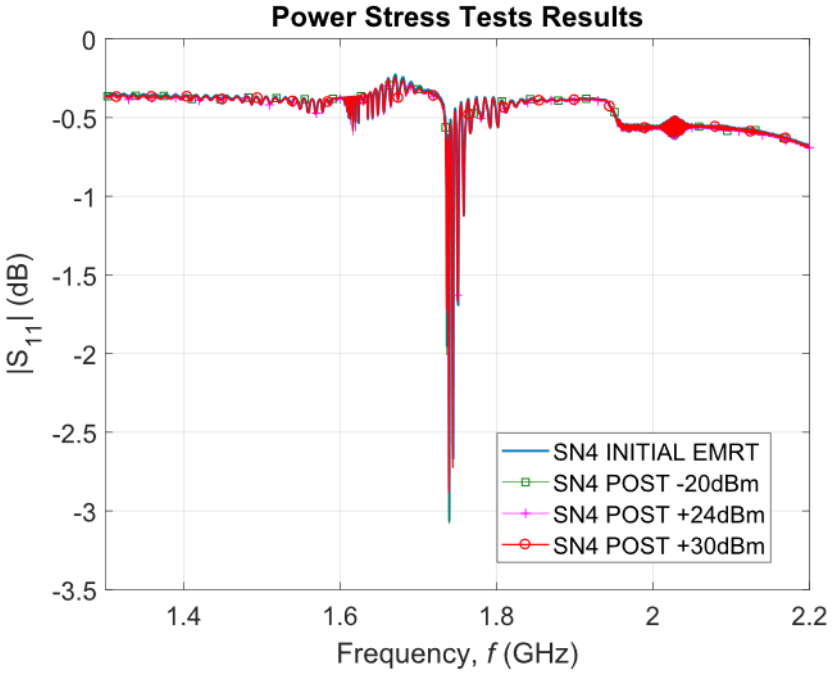


Fig 9. S11 measurements during power step-stress testing, shown for the initial step (blue), post -20dBm (square), post +24dBm (+), and final measurements post +30dBm (circle)

The nearly overlapping S11 responses indicate stable performance under increasing RF power stress. Finally, the same procedure used to extract parameter values at each step of the TST was also applied in this case. After the S_{11} measurements were completed, the de-embedding process was performed using open and short standards.

CONCLUSIONS AND PERSPECTIVES

The evaluation presented in this work was conducted within the framework of a stress-based assessment methodology aimed at identifying potential failure modes in optimized POI-based SAW resonators under progressively increasing thermal and RF excitation conditions. The primary objective of the test campaign was to overstress specific device characteristics to detect possible failure mechanisms and assess the robustness limits of the technology under representative environmental conditions. In addition, the applied methodology is intended to support future failure analysis activities in the event of device malfunction, enabling the identification of potential design, material, or fabrication-related weaknesses.

The results obtained from both Temperature Step Stress (TST) and Power Step Stress (PST) testing indicate that all tested devices remained operational throughout the full stress sequence, with no observed failures or evidence of degradation within the applied test limits.

The S_{11} responses remained highly consistent across all stress steps, and the extracted resonator parameters showed stable behavior within the expected measurement uncertainty, confirming repeatable device performance under stress conditions. From a reliability perspective, no failure modes were triggered during the evaluation, and no anomalous behavior was observed that would indicate intrinsic weaknesses under the tested conditions.

These findings provide a first indication of the robustness of the current new POI resonator design under combined thermal and RF stress and support its continued investigation. Future activities will focus on extending the sample population, refining stress margins, and progressing toward filter-level implementations and higher TRL qualification campaigns, including dedicated failure analysis when applicable.

ACKNOWLEDGMENTS

This work was carried out within the framework of the HOMEMADE project funded by the European Union (HORIZON EUROPE, No. 101081785, Horizon-CL4-2021-SPACE-01). We thank all project participants for their valuable contributions and collaboration, which were essential to the success of this work, with special recognition to the SOITEC Innovation Group for its key role and contributions in the fabrication of standard and advanced POI wafers. We also gratefully acknowledge the SOITEC team for providing the highest-quality wafers, and especially Frederic Allibert, Marcel Broekaert, and Luciana Cappello for their important contributions to the development of the new rap-Rich POI.

REFERENCES

[1] E. Butaud et al., ‘A Single Smart Cut POI Substrate Design for UHF, L and S Band Filters’, in 2020 50th EuMC), 2021, pp. 654–657[Online]. Available: 10.23919/EuMC48046.2021.9338169.

[2] X. Seah et al., "High Q-Factor Low Band SAW Filter Based on High Performance POI Substrate," 2024 IEEE MTT-S International Conference on Microwave Acoustics & Mechanics (IC-MAM), Chengdu, China, 2024, pp. 125-128, doi: 10.1109/IC-MAM60575.2024.10538490

[3] ESCC Basic Specification No. 2263502, “EVALUATION TEST PROGRAMME FOR SURFACE ACOUSTIC WAVE (SAW) DEVICES”.

[4] ESCC Generic Specification No. 3502 for SURFACE ACOUSTIC WAVE (SAW) FILTERS, HERMETICALLY SEALED.

[5] M. Rack, F. Allibert, J-P. Raskin, "Modeling of Semiconductor Substrates for RF Applications: Part I—Static and Dynamic Physics of Carriers and Traps," IEEE Trans. on Electron Devices, vol. 68, no. 9, pp. 4598-4605, Sept. 2021, doi: 10.1109/TED.2021.3096777

[6] S.Ballandras & al, Spurious signal control for SAW devices on POI substrates, Proc. of the IEEE IC-MAM 2026, unpublished.

AUTHORS



Kaoutar Zeljami was born in Tetuan, Morrocco. She received her Ph.D. from the University of Cantabria, Spain, in 2013, where her research focused on the characterization and modelling of semiconductor devices at terahertz frequencies, particularly Schottky diodes.
She has participated in several research projects in microwave and terahertz technologies and has extensive experience in the characterization, testing, screening, and qualification of RF components. After working as a Research Engineer at BlueICe, Belgium, she joined Alter Technology in January 2023, where she is currently a Microwave Engineer and Coordinator of the RF and Microwave Group, testing, screening, and qualification activities for radio-frequency devices used in space and industrial applications.



Aintzane Lujambio Genua obtained the Telecommunication engineering degree and Ph.D. in Communications in the Public University of Navarre in 2006 and 2014 respectively. She participated in several research activities focused on the design and characterization of microwave components as part of the Microwave Components Group of the Public University of Navarre, and afterwards with the Microwave Group of the University of Seville, in the Department of Electronic and Electromagnetism. She joined Alter Technology Tüv Nord in 2017 as development engineer for microwave components. With an experience of more than 10 years in the microwaves industry, she is working at the EEE parts laboratory department as head of the Microwave Laboratory. She has been involved in testing activities such as screening and qualification microwave components for different space missions such as ESA's JUICE mission.



Sylvain Ballandras (Senior member, IEEE) was born in Strasbourg, France, in 1965. He received his PhD in 1991 and his Habilitation à Diriger les Recherches in 1997, both from the University of Franche-Comté. He joined the CNRS in 1991, working on SAW devices and on micro-machining. He participated in a joint laboratory between Thomson Microsonics and CNRS. He joined this company from 1997 to 1998. He was promoted Research Director at the CNRS in 2003. In 2004, he created his consulting office. In 2006, he was involved in the creation of SENSeOR as scientific adviser from 2009 to 2012. In 2013, he created frec|n|sys, a company devoted to acoustic wave devices acquired by SOITEC and integrated in 2017 and 2023. Sylvain Ballandras is an IEEE-UFFC senior member. He was elected member of the IEEE UFFC AdCom for the period 2011-2014. He received the Cady award in 2022.



Thierry Laroche received the Ph.D. degree in nano-optics from the University of Franche-Comté, Besançon, France. He subsequently completed a postdoctoral fellowship in nanoscience at the Center for Material Elaboration and Structural Studies (CEMES) in Toulouse, France, where he coordinated European research initiatives on plasmo-nanodevices. In 2006, he was appointed Assistant Professor of nanotechnology at the University of Technology of Troyes (UTT), France. He later spent six years with the FEMTO-ST Institute, Besançon, focusing on time and frequency applications, before joining frec|n|sys SASU in 2013 as the Head of the Design and Modeling team. Following Soitec's acquisition of frec|n|sys, he transitioned to Soitec, where he currently leads advanced design and simulation activities for the development of next-generation POI wafers and filter-on-POI products.



Emilie Courjon was born in 1981. She obtained the "Diplôme d'Ingénieur" from the Institut Supérieur d'Ingénieur de Franche Comté in 2004. She obtained her PhD in 2009, working on ferroelectric transducers for radio-frequency filtering and signal processing applications. She then has been working in the technological platform of the FEMTO-ST Institute since 2009 till 2013 where she was in charge on the so-called exogenous projects supervising all the technology developments and achievements of the company. She joined frec|n|sys as Production Manager in 2013, a company devoted to acoustic wave devices acquired by SOITEC and integrated in 2017 and 2023. Her skills are in the field of photolithography process, SAW device manufacturing, characterization and piezoelectric material related technology.



Florent Bernard has received his PhD from University of Franche-Comté. He has worked for CNRS since 2008 in the materials and thin film fields. He joined frec|n|sys in 2015 as a microtechnologic engineer for acoustic waves device fabrication. Integrated by Soitec in 2023, he is acting as technological leader in the POI & Design Filter Business Line.



Alexandre Raveski received his Licence Professionnelle MPPN Micro Procédés Process Numérique from the University Institute of Technology (IUT) of Besançon, France on work-study program at frec|n|sys in 2014. He worked on developing a high temperature sensor, wire bonding, devices assembly and 3D design. He joined frec|n|sys in 2015 and subsequently Soitec in manufacturing within the POI & Design Filter Business Line as a front-end and back-end technician.